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- $1$ .	An apparatus,	comprising

- a) a backplane, said backplane having a switch card interface and an
  adapter card interface;
- b) said switch card interface having input/outputs in an arrangement that functionally mates to a networking layer system switch card and a physical layer system switch card; and
  - c) said adapter card interface coupled to said switch card interface, said adapter card interface having input/outputs in an arrangement that functionally mates to a networking layer system adapter card and a physical layer system adapter card.
- The apparatus of claim 1 further comprising a processor card interface, said
  processor card interface coupled to said switch card interface and said
- 3 adapter card interface.
- The apparatus of claim 2 wherein said coupling between said processor card
  interface and said switch and adapter card interfaces further comprises a
- 3 system bus.

- 1 4. The apparatus of claim 2 wherein said coupling between said processor card
- 2 interface and said switch and adapter card interfaces further comprises a
- 3 clock trace.
- 5. The apparatus of claim 4 wherein said clock line connects said processor
- 2 card interface to said adapter card interface.
- 1 6. The apparatus of claim 4 wherein said clock line connects said processor
- 2 card interface to said switch card interface.
- 7. The apparatus of claim 1 wherein said coupling further comprises a major
- 2 link, said major link comprising at least one minor link.
- 1 8. The apparatus of claim wherein said minor link further comprises a pair of
- 2 differential transmit traces.
- 9. The apparatus of claim 7 wherein said minor link further comprises a pair of
- 2 differential receive traces.
- 1 10. The apparatus of claim 1 further comprising an ATM switch card mated
- 2 with said switch card interface and an ATM adapter card mated with said
- 3 Adapter card interface.

- 1 13. The apparatus of claim 12 further comprising an ATM switch card mated
- 2 with one of said switch card interfaces and a SONET switch card mated
- 3 with another of said switch card interfaces.
- 14. The apparatus of claim 13 further comprising an ATM adapter card mated 1
- 2 with one of said adapter card interfaces and a SONET adapter card mated
- 3 with another of said adapter card interfaces.

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15. The apparatus of claim 13 further comprising a hybrid adapter card mated

- with one of said adapter card interfaces, each of said adapter card interfaces
- 3 having input/outputs that functionally mate to said hybrid adapter card.
- 1 16. The apparatus of claim 12 further comprising a first ATM switch card mated
- with one of said switch card interfaces, a redundant ATM switch card mated
- with another of said switch card interfaces and an ATM adapter card mated
- 4 with one of said adapter card interfaces.

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17. The apparatus of claim 16 wherein said coupling further comprises a

- plurality of major links, one major link between each said adapter card and
- 3 each said switch card, each of said major links further comprising a plurality
- 4 of minor links, each of said minor links further comprising a real data minor
- 5 link and a redundant minor link.
- 1 18. The apparatus of claim 12 further comprising a first SONET switch card
- 2 mated with one of said switch card interfaces, a redundant SONET switch
- 3 card mated with another of said switch card interfaces and a SONET
- 4 adapter card mated with one of said adapter card interfaces.

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19. The apparatus of claim 18 wherein said coupling further comprises a

2 plurality of major links, one major link between each said adapter card and

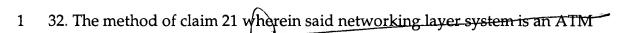
- 3 each said switch card, a real data major link between said SONET adapter
- 4 card and said first SONET switch card, a redundant major link between said
- 5 SONET adapter card and said redundant SONET switch card.

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- 20. The apparatus of claim 12 further comprising four said switch card
- 2 <u>interfaces</u> and twelve said adapter card interfaces.
- 1 21. A method, comprising:
- a) forming a first and second backplane according to a manufacturing
- 3 process;
- b) integrating said first backplane into a networking layer system; and
- 5 c) integrating said second backplane into a physical layer system.
- 1 22. The method of claim 21 wherein said manufacturing process further
- 2 comprises forming minor link conducting traces associated with a major
- 3 link.
- 1 23. The method of claim 22 wherein said forming minor link conducting traces
- 2 further comprises forming a pair of differential transmit conducting traces.
- 1 24. The method of claim 23 wherein said forming minor link conducting traces
- 2 / further comprises forming a pair of differential receive conducting traces.

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- 1 25. The method of claim 21 wherein said manufacturing process further
- 2 comprises forming system bus conducting traces.
- 1 26. The method of claim 21 wherein said manufacturing process further
- 2 comprises forming clock traces.
- 1 27. The method of claim 21 further comprising affixing a card interface to said
- 2 backplane.
- 1 28. The method of claim 27 further comprising affixing an adapter card
- 2 interface to said backplane.
- 1 29. The method of claim 27 further comprising affixing a switch card interface
- 2 to said backplane.
- 1 30. The method of claim 27 further comprising affixing a processor card
- 2 interface to said backplane.
- 1 31. The method of claim 21 wherein said manufacturing process further
- 2 /comprises a lithographic process that employs a mask set.



2 switch and said physical layer system is a SONET switch.

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